corresponding to shared connections between some gate electrodes groups to the connection terminals within said successive pixel rows and a maximum number corresponding to one half the number of pixels in a column, being combined with N gate electrode groups to reduce the number of the connection terminals.

B6 cont.

In accordance with 37 C.F.R. § 1.121(c)(1)(ii), a separate sheet(s) with the rewritten claims marked-up to show the changes made to the previous version of the claims, is filed herewith.

IN THE DRAWINGS:

Proposed drawing corrections to Figures 6 and 7 are filed herewith for the Examiner's approval. In accordance with 37 C.F.R. § 1.121(d), separate sheets marked up in red to show all changes, is filed herewith.

**REMARKS**

In view of the foregoing amendments and the following remarks, the applicants respectfully submit that the pending claims are not anticipated under 35 U.S.C. § 102, and are definite under 35 U.S.C. § 112 ¶ 2. Accordingly, it is believed that this application is in condition for allowance. If, however, the Examiner believes that there are any unresolved issues, or believes that some or all of the claims are not in condition for allowance, the applicants respectfully request that the Examiner contact the undersigned to schedule a telephone

Examiner Interview before any further actions on the merits.

The applicants will now address each of the issues raised in the outstanding Office Action.

**Drawings**

Figures 6 and 7 are objected to by the Examiner as not including a "Prior Art" legend. Proposed revisions to these drawings to add such a "Prior Art" legend are filed herewith.

**Objections**

Claims 1, 2, 4 and 5 are objected to by the Examiner because of various minor informalities. The applicants have amended claims 1, 2, 4 and 5 based on the Examiner's helpful suggestions. Therefore, the applicants request that the Examiner reconsider and withdraw the objections in view of the amendments made to the claims.

**Rejections under 35 U.S.C. § 102**

Claims 1-9 stand rejected under 35 U.S.C. § 102 as being anticipated by the prior art discussed in the application. The applicants respectfully request that the Examiner reconsider and withdraw this ground of rejection in view of the following.

Independent claims 1, 2, 4 and 5 are not anticipated by the purported prior art discussed in the

application because the purported prior art does not teach gate electrodes within successive pixel rows belonging to each coset of modulo N, where N is a predetermined natural number between 4 and one half the number of pixels in a column, and a minimum number of N corresponding to a periodic unit of gate electrode connections to connection terminals within the successive pixel rows. Claim 1, as amended is reprinted below with this feature depicted in bold face:

> 1. (AMENDED) A solid-state imaging device comprising:
>
> a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;
>
> a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;
>
> shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and
>
> a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit,
>
> **the gate electrodes within successive pixel rows belonging to each coset of modulo N, N being a predetermined natural number between 4 and one half the number of pixels in a column, and a minimum number of N corresponding to a periodic unit of gate electrode connections to said connection terminals within said**

> **successive pixel rows**, the gate electrodes being combined with N gate electrode groups to reduce the number of the connection terminals. [Emphasis added.]

Independent claims 2, 4 and 5 have been amended to include a similar recitation. Therefore those claims include features that are not taught by the purported prior art discussed in the application.

Before discussing the above-noted feature of the claimed invention, it may be helpful to review the exemplary embodiment of the invention depicted in Figure 3. In Figure 3 the leftmost column of boxes 1 represents one column of pixels from a two-dimensional pixel unit. (See, e.g., page 11, lines 28-29.) The pixels are grouped into pixel groups of 16 pixels. Each pixel has two corresponding electrodes within a vertical transfer path 2. (See, e.g., page 12, lines 7-9.) For example, pixel number 3 corresponds to electrodes 3a and 3b. Each of the "a" electrodes are coupled with the pixels via shift gates 3. (See, e.g., page 12, lines 9-13.) Therefore the "a" electrodes may be used to control the shifting of a charge from a pixel to the vertical transfer path 2. The "a" electrodes are also used to transfer a charge along the vertical transfer path 2, e.g., when it is time for a CCD to read out the charges corresponding to a picture. (See, e.g., page 4, lines 17-20.) For clarity, the "a" electrodes will be referred to as "gate electrodes", although the "a" electrodes also include transfer abilities and may be called transfer electrodes in other situations. The "b" electrodes are used to transfer charge along the vertical transfer path 2. (See, e.g., page 13, lines 8-10.)

Therefore the "b" electrodes will be referred to as "transfer electrodes". Electrodes of the same number and letter define an electrode group. For example, each of the 1a electrodes define an electrode group, each of the 1b electrodes define another electrode group, each of the 2a electrodes define yet another electrode group, and so on. The rightmost column of circles 6 represents connection terminals to an external circuit (e.g., for controlling the gate electrodes). (See, e.g., page 5, lines 3-6.)

In at least one part of the present invention, gate electrodes within successive pixel rows each belong to a coset of modulo N. N is a predetermined natural number between 4 and one half the number of pixels in a column, and a minimum value of N corresponds to a periodic unit of gate electrode connections to the connection terminals within successive pixel rows. Therefore the minimum value of N is determined corresponding to how gate electrodes are coupled to connection terminals.

The way this feature patentably distinguishes the invention over the prior art can be appreciated by comparing Figures 3 (one embodiment of the invention) and 7 (the purported prior art). In Figure 7, each of the group "a" gate electrodes belonging to a pixel group of 16 pixels has its own individual connection terminal to external circuits. (See, e.g., page 4, lines 22-24.) In other words **each gate electrode group has its own exclusive connection terminal**. In contrast, an exemplary embodiment of the present invention, shown in Figure 3, shows some of the group "a" gate electrodes belonging to a pixel group of 16 pixels **sharing a connection to a connection terminal**.

(See, e.g., in Figure 3, gate electrodes 2a and 4a of the same pixel group sharing connection terminal 2.) These shared connections may be repeated periodically throughout the rest of the pixel groups. Note that the sharing of connection terminals is not limited to the example of Figure 3, and several different connection configurations may be used. Therefore the minimum value of N may be affected by the periodic gate electrode connections to connection terminals.

The purported prior art of Figure 7 does not teach gate electrodes, within a given pixel group, sharing a connection terminal, let alone a number N that may have a minimum value corresponding to a periodic unit of gate electrode connections to connection terminals. Stated differently, Figure 7 does not teach sharing connection electrodes by electrodes from different gate electrode groups.

As discussed in the application, the example illustrated in Figure 7 has a large number of lead lines and external circuit connections (See page 5, lines 16-21). Unfortunately, this leads to higher productions costs and materials costs. Since the purported prior art does not teach a number N that is between 4 and one half the number of pixels in a column, and a minimum number of N corresponding to a periodic unit of gate electrode connections to connection terminals within the successive pixel rows, claims 1, 2, 4 and 5 are not anticipated by the purported prior art for at least this reason. Since claims 7 and 8 depend from claims 4 and 5, respectively, these

claims are similarly not anticipated by the purported prior art disclosed in the application.

Independent claims 3 and 6 are not anticipated by the purported prior art discussed in the application because the purported prior art does not teach gate electrodes groups being commonly connected so that the number of connection terminal is less than the number of electrode groups. Claim 3, as amended is reprinted below with this feature depicted in bold face:

> 3. (Amended) A solid-state imaging device comprising:
>
> a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;
>
> a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;
>
> shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and
>
> a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit,
>
> the gate electrodes being provided in a predetermined number N, N being a predetermined natural number between 4 and one half the number of pixels in a column, of gate electrode groups such that horizontal line number of the gate electrode groups which are connected to respective common lead lines belong to

each same residue class of modulo N, **some of the gate electrode groups being commonly connected so that the connection terminals are less in number than N.** [Emphasis added.]

Independent claim 6 includes a similar recitation.

The Examiner may not have appreciated the difference between gate electrodes and transfer electrodes. To reiterate, in Figure 3, the vertical transfer path 2 includes two electrodes for each pixel. The "a" electrodes are referred to as gate electrodes, because they may be used to control the shift gates and they are used for transferring charge along the vertical transfer path 2, and the "b" electrodes are referred to as transfer electrodes, because they are used for transferring charge along the vertical transfer path 2. Please note that the patentable feature of claim 3 recites gate electrodes. In addition, the Examiner may also not have appreciated the definition of a gate electrode group. A gate electrode group comprises, e.g., each of the 1a gate electrodes in different pixel groups, each of the 2a gate electrodes in different pixel groups, and so on. This is expressed in claim 3 as follows. Claim 3 defines gate electrode groups such that a horizontal line number of the gate electrode groups which are connected to respective common lead lines belong to each same residue class of modulo N.

The Examiner argues that the purported prior art teaches a solid-state imaging device comprising 16 connection terminals for 32 gate electrode groups of 2 pixels each, i.e., having less connection terminals than gate electrode groups. (See paper No. 5, page 5.) This is

incorrect. An exemplary solid-state imaging device having 32 gate electrode groups would have 2 pixel groups of 32 pixels each and would have 32 connection terminals. Page 4, lines 20-27, recites that independent gate pulse application lead lines should be provided to the electrodes 1a to 16a. Therefore according to the discussion of Figure 7, an exemplary solid-state imaging device having 32 gate electrode groups would have exactly one corresponding connection terminal for each of the gate electrode groups, for a total of 32, not 16, connection terminals. Therefore the solid-state imaging device proposed by the Examiner would not have less connection terminals than gate electrode groups. Accordingly, claims 3 and 6 are not anticipated by the purported prior art of at least this reason.

In other words, note that the examples illustrated in Figures 3 and 7 both include 16 gate electrode groups. Referring to Figure 7, each of the 1a gate electrodes share a connection terminal, but none of the gate electrode groups share a connection terminal (i.e., there are 16 connection terminals for 16 gate electrode groups). In contrast, referring to Figure 3, notice that some gate electrode groups share a connection terminal, e.g., gate electrode groups 2a and 4a. The sharing of connection terminals by gate electrode groups allow there to be 12 connection terminals for 16 gate electrode groups. As recited in claim 3, some gate electrode groups are commonly connected so that the connection terminals (e.g., 12) are less in number than the number of gate electrode groups (e.g., 16). Since the purported prior art does not teach having less connection

terminals than gate electrode groups, claims 3 and 6 are not anticipated by the purported prior art for at least this reason. Since claim 9 depends from claim 6, this claim is similarly not anticipated by the prior art disclosed in the application.

**Rejections under 35 U.S.C. § 112**

Claims 2, 3, 5 and 6 stand rejected as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. The applicants have amended these claims to provide sufficient antecedent basis for the elements identified by the Examiner. Therefore the applicants request that the Examiner reconsider and withdraw these rejections in view of the amendments to the claims.

**New claim**

New independent claim 10 further recites the sharing of connection terminals between gate electrode groups to minimize the number of connection terminals and lead lines. Support for new claim 10 is described on page 12, line 27 through page 13, line 8, and shown in Figure 3.

**Conclusion**

In view of the foregoing amendments and remarks, the applicant respectfully submits that the pending claims are in condition for allowance. Accordingly, the

applicants request that the Examiner pass this application to issue.

Respectfully submitted,

April 15, 2002

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**CERTIFICATE OF MAILING under 37 C.F.R. 1.8(a)**

I hereby certify that this correspondence is being deposited on **April 15, 2002** with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

John C. Pokotylo — Reg. No. 36,242

**SEPARATE SHEETS WITH MARKED-UP VERSION OF CHANGES TO THE SPECIFICATION IN ACCORDANCE WITH 37 CFR § 1.121(b)(2)(iii)**

The paragraph starting at page 1, line 11 has been amended as follows:

Recently, development of so-called electronic still cameras, which are electronic imaging apparatuses capable of inputting image data to multi-media systems, is in force. The electronic still camera usually uses a solid-state imaging unit, such as a CCD imaging device, for obtaining images. The image obtained in such a camera is displayed on a liquid crystal panel of like view-finder, and can also be recorded in a recording medium in response to the depression of a trigger by the user. It has been demanded to further improve the image quality and operation control property of the electronic camera. To meet these demands it is indispensable to use a CCD imaging device having a large number of pixels and also that it is desirable to real time confirm image of the same view angle as picked-up image with a view-finder.

The paragraph starting at page 2, line 15 has been amended as follows:

Fig. 6 shows a construction which is conceivable in the case where the interlace system is applied to the usual inter-line type CCD imaging device. This example is of four-phase drive type with a least recurrence unit of two pixels. For the sake of the brevity, 16 pixels are shown as a set. These sets of pixels are arranged successively

one after another in the vertical direction of vertical transfer path. In the Figure, reference numerals 1 to 16 within rectangles each designate each pixel 1. A vertical transfer path 2 has two groups a and b of vertical transfer electrodes 1a, 1b to 16a, 16b. Two like sequence transfer electrodes in the two electrode groups are provided for each of the pixels in each set. Each pixel 1 is connected via a shift gate 3 to each transfer channel in the vertical transfer path 2 corresponding to each of the transfer electrodes 1a to 16a in the electrode group a. The vertical transfer electrodes are connected to corresponding ones of four shift pulse application lead lines 4, via which 4-phase shift pulses out of phase by 1/4 cycle with one another are applied. The 4-phase transfer pulses are successively applied to the transfer electrodes, which are grouped in groups each of four transfer electrodes, whereby the charge read out via the shift gates to the vertical transfer path 2 are transferred in one direction. In Fig. 6, reference numeral 5 designates connection electrodes for connecting the lead lines 4 to an external circuit.

The paragraph starting at page 10, line 4 has been amended as follows:

Referring to the Figure, reference numeral 11 designates a single plate color CCD imaging device, which photoelectrically converts light to an electric signal and has an electronic shutter function. A scene light flux can be inputted through a lens 12 and a stop-shutter mechanism 13 to the CCD imaging device 11. The output of the CCD imaging device 11 is subject to noise removal and amplification in a pre-processor 14, which includes a

correlated double-sampling circuit and a pre-amplifier. An A/D converter 15 converts the output of the pre-processor 14, inputted as analog data, to digital data. A camera signal processor 16 processes the signal from the CCD imaging device 11 as image data. An AF/AE/AWB detector 17 includes an AF detector for generating AF data for focus control on the basis of the image signal from the CCD imaging device 11 prior to the intrinsic photography, an AE detector for generating AE data for exposure control and an AWB detector for generating an AWB data for white balance level setting. The AF, AE and AWB data from the AF/AE/AWB detector 17 are supplied through a CPU 18 to the lens 12, the stop/shutter mechanism 13 (via stop/shutter driver 29) and the camera signal processor 16, respectively.

The paragraph starting at page 11, line 28 has been amended as follows:

Fig. 3 partly shows a single vertical pixel [row]column and a vertical transfer path 2 corresponding thereto. Like the CCD imaging device shown in Fig. 6, this CCD imaging device has a plurality of pixel groups 1, which are each constituted by 16 pixels in successive vertical arrangement and are [arranged] successively arranged vertically along a vertical transfer path 2. The vertical transfer path 2 has two groups a and b of transfer electrodes 1a, 1b to 16a, 16b. Two like sequence transfer electrodes in the two electrode groups a and b are provided for each of the pixels 1 in each set. Each pixel 1 is connected via a shift gate 3 to each transfer channel in the vertical transfer path 2 corresponding to each of the transfer electrodes 1a to 16a in the electrode group a in

the vertical transfer path 2. To the transfer electrodes 1a to 16a of the electrode group a, independent shift/transfer pulse application lead lines 4A are connected to permit gate pulse application and also independent gate pulse application to the shift gates. The respective pixels of the same order in the successively arranged pixel groups each of 16 pixels, that is, the line pixel corresponding to each coset of modulo 16, are connected to an independent shift/transfer pulse application common lead line. The number of the pixels in each of the successively arranged pixel groups is usually set to 8, 16, etc., but theoretically it may be a natural number between 4 and one half the number of pixels in each column.

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**SEPARATE SHEETS WITH MARKED-UP VERSION OF CLAIMS PER 37 C.F.R § 1.121(c)(1)(ii)**

1. (Amended) A solid-state imaging device comprising:

a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;

a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and

a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit,

the gate electrodes within successive pixel rows belonging to each coset of modulo N, [()]N being a predetermined natural number between 4 and one half the number of pixels in a column, and a minimum number of N corresponding to a periodic unit of gate electrode connections to said connection terminals within said successive pixel rows, [()] the gate electrodes being combined with N gate electrode groups to reduce the number of the [external] connection terminals.

2. (Amended) A solid-state imaging device comprising:

a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;

a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and

a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit,

[the] gate control lines within successive pixel rows belonging to each coset of modulo N, [()]N being a predetermined natural number between 4 and one half the number of pixels in a column, and a minimum number of N corresponding to a periodic unit of gate electrode connections to said connection terminals within said successive pixel rows, [()] being combined with each other so as to reduce the number of the [external] connection terminals.

3. (Amended) A solid-state imaging device comprising:

a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;

a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and

a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit,

the gate electrodes being provided in a predetermined number N, [()]N being a predetermined natural number between 4 and one half the number of pixels in a column, [)] of gate electrode groups such that horizontal line number of the gate electrode groups which are connected to respective common lead lines belong to each same residue class of modulo N, some of the gate electrode groups being commonly connected so that the connection terminals [electrodes] are less in number than N.

4. (Amended) A solid-state imaging device comprising: a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time; a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit, the gate electrodes within successive pixel rows [belong] belonging to each coset of modulo N, [()]N being a predetermined natural number between 4 and one half the number of pixels in a column, and a minimum number of N corresponding to a periodic unit of gate electrode connections to said connection terminals within said successive pixel rows,[)] the gate electrodes being combined with N gate electrode groups to reduce the number of the [external] connection terminals,

wherein the commonly connected gate electrode groups are always controlled in the same way in each of all predetermined read-out modes including selective pixel read-out modes by selective shift gate driving.

5. (Amended) A solid-state imaging device comprising: a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time; a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit; shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the

pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit, [the] gate control lines within successive pixel rows [belong] belonging to each coset of modulo N, [(]N being a predetermined natural number between 4 and one half the number of pixels in a column, and a minimum number of N corresponding to a periodic unit of gate electrode connections to said connection terminals within said successive pixel rows,[)] being combined with each other so as to reduce the number of the [external] connection terminals,

wherein the commonly connected gate electrode groups are always controlled in the same way in each of all predetermined read-out modes including selective pixel read-out modes by selective shift gate driving.[.]

6. (Amended) A solid-state imaging device comprising: a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time; a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit; shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and a plurality of lead

lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit, the gate electrodes being provided in a predetermined number N, [(]N being a predetermined natural number between 4 and one half the number of pixels in a column,[)] of gate electrode groups such that horizontal line number of the gate electrode groups which are connected to respective common lead lines belong to each same residue class of modulo N, some of the gate electrode groups being commonly connected so that the connection terminals [electrodes] are less in number than N,

wherein the commonly connected gate electrode groups are always controlled in the same way in each of all predetermined read-out modes including selective pixel read-out modes by selective shift gate driving.

10. (New) A solid-state imaging device comprising:

a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;

a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and

a plurality of lead lines and a plurality of connection terminals for connecting the gate electrodes to an external circuit,

the gate electrodes within successive pixel rows belonging to each coset of modulo N, N being a predetermined natural number between a minimum number corresponding to shared connections between some gate electrodes groups to the connection terminals within said successive pixel rows and a maximum number corresponding to one half the number of pixels in a column, being combined with N gate electrode groups to reduce the number of the connection terminals.